CLAIMS

1. A versatile and programmable Smart Power IC, to provide switching power cells, their drives and protections and other required circuits to control, amplify and sample output variables to meet a wide range of applications requirements, characterized by:

a) comprising Arrays aimed at Power Integrated Circuits (PICs), containing "intelligence" or not, based on the association of NMOS FETs, wherein said, NMOS structures, using a specific layout in a simple pattern, enabling to perform different functions required by Smart Power ICs;

b) providing novel circuit Topologies to enable the control and power signals processing of PICs resorting only to wherein said NMOS structures in association with passive components within the same monolithic circuit or external to it;

c) using wherein said NMOS based Basic Cells, which make use of an association of FETs, such as LDD or LDSD-NMOS or both, or LDMOS or N channel DMOS.

2. A Smart Power IC as defined in claim 1 implemented by wherein said Mask Programmable Smart Power Array by means of:

a) top metal masks layout, which define the semi-custom array NMOS structures interconnections;

b) novel Topologies of the required circuits aimed at power signals proccessing, using wherein said NMOS structures associations interconnected to define specific functions to be added in Cell libraries, to be used towards a wide range of applications; and

c) complete mask layout to define the NMOS based elementary associations, that support system built-up.

3. A Smart Power IC as defined in claim 1, the circuits topologies of which are obtained through appropriate configuration of the wherein said Mask Programmable Smart Power Array as defined in claim 2. These circuits include:

a) said rectifiers and wherein said programmable "Zeners", required in NMOS based clippers and clampers;

b) wherein said NMOS based level-shifter;

c) wherein said NMOS based charge-pump; and

d) wherein said NMOS based bootstrap;

e) wherein said NMOS based current source;

including appropriate design methodologies and simulation models.

4. A Smart Power IC as defined in claim 1, characterised by elementary associations, only resorting to a set of NMOS transistors either of LDD or LDSD type, or both, or LDMOS or DMOS, which include:

a) flexible interconnection of the whole set of NMOS structures terminals;

b) a P^+ guard ring connected to the substrate, involving the elementary cell;

c) connection of LDD type transistors Sources to the referred guard ring;

d) floating LDSD and LDMOS type transistors Sources;

e) specific layout to:

- permit local interconnections of Drain, Gate and Source terminals;

- make easy the implementation of interconnections through columns between the elementary cells; and

- make easy the association of elementary cells in order to obtain more complex circuits, through appropriate interconnections.

5. Smart Power Applications resorting to the Array as defined in claims 1 and 2, incorporating "intelligence" or not, and to the novel topologies as defined in claims 2 and 3 to obtain required: power control, switching and their drives; sampling and protection; towards power conversion and amplification. These arrays can be fabricated either in standard CMOS technology or other CMOS technologies that require additional process steps or yet sophisticated Power Integration technologies or specific Smart Power technologies. These arrays can be configurated in order to perform a large set of functions as defined in claim 3, according to methodologies as defined in claim 4, which are able to associate multiple NMOS transistors in specific configurations, in association with passive elements, integrated or not, to permit:

- the implementation of a large set of power switching cells presenting different switch topologies – high-side; low-side; pass element; push-pull; half-bridge; full-bridge, n-phases-bridge and other derived topologies;

- the implementation of different devices and circuits required for driving the different power switching topologies;

- the implementation of sampling and protection circuits required to achieve a good performance of the power switching cells;

- to increase the robustness of smart power ICs with respect to electrostatic discharges and latch-up behaviour; and

- the fast prototyping of Smart Power circuits and Microsystems.

6. LDD and LDSD type, N channel, Metal-Oxide-Semicondutor Field Effect Transistors, wherein said Gate-Shifted Lightly Doped Drain - GSLDD and wherein said Gate-Shifted Lightly Doped Source and Drain -

GSLDSD, which resort to the wherein said gate-mask shift with respect to N-well mask edge to enlarge breakdown voltage and thus, to expand the application range of wherein said Mask Programmable Smart Power Array as defined in claims 1, 2, 3, 4 and 5, comprising:

- fully standard CMOS (N-well, P substrate, one polysilicon layer and at least two metal layer) compatible;

- a lateral planar configuration for the wherein said GSLDD, with the said Drain formed by a high impurities concentration diffusion embbeded in the low doping concentration N-well;

- a connection between said substrate and said source terminals for the wherein said GSLDD;

- specific mask layout that allows the said GSLDD drain to handle high voltages;

- a lateral planar configuration for the wherein said GSLDSD, with said Drain and Source formed by high impurities concentration diffusions embbeded in low doping concentration N-wells;

- said source terminals isolated from the said substrate for the wherein said GSLDSD;

- specific mask layout that allows both said GSLDSD drain and source to handle high voltages;

- the use of the wherein said gate-shifted technique, to obtain the alignment of the said gate mask with the said N-well lateral diffusion periphery path, taking advantage of reduced surface electric field maximum values inherent to low impurities concentration regions, thus increasing device maximum voltage rating.